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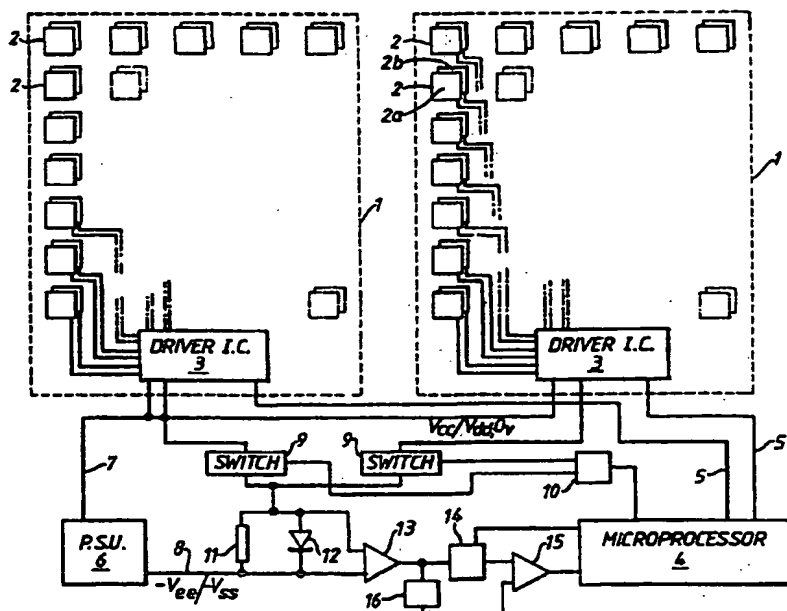
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(54) Title: FAULT DETECTION ARRANGEMENT FOR A LIQUID CRYSTAL DISPLAY



(57) Abstract

A fault detection arrangement is disclosed for a liquid crystal display element having a pair of opposed electrodes across which an a.c. driving signal is applied. The arrangement comprises means for increasing the frequency of the driving signal and for comparing the current flowing between the electrodes with a predetermined value.

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FAULT DETECTION ARRANGEMENT FOR A LIQUID CRYSTAL DISPLAY

This invention relates to a fault detection arrangement for use with a liquid crystal display and is particularly suited for use with displays of the type comprising large arrays of LCD shutters which can be selectively switched to mask and unmask a light source.

Such displays are becoming more popular for use as road signs to display information of a variable nature. A need exists for a fault detection arrangement which can be built into the control system for such a display and which can periodically test for the presence of faults within the various LCD elements.

This invention provides a fault detection arrangement for a liquid crystal display element having a pair of opposed electrodes across which an a.c. driving signal is applied, the arrangement comprising means for increasing the frequency of the driving signal and for comparing the current flowing between the electrodes with a predetermined value.

The invention is based upon the appreciation that each LCD element has an intrinsic capacitance and, as such, draws a certain current when driven with a certain frequency and voltage waveform. A fault due to a full or partial short or open circuit will lead to a change in the drawn current. However at the frequencies with which such displays are typically driven the currents are of very small magnitude as compared to the currents flowing around the associated driving circuitry. A further problem arises

due to the fact that, with the semiconductor driving circuits currently available, the quiescent currents - i.e. those currents flowing when no liquid crystal elements are energised - are not particularly stable and vary with operating temperature. These problems can be overcome if the driving frequency is increased as this leads to larger currents which can be more easily detected.

It is preferred that the means is operative to progressively change the frequency over a range of values so as to account for component tolerances and ensure that a correctly functioning display passes a current corresponding to the predetermined value at one frequency within the range. Preferably the range is selected such that a fault due to a full or partial short circuit between the electrodes is signalled upon detection of a current higher than the predetermined value at the lowest driving frequency, and a full or partial open circuit fault, between the electrode interconnections for example, is signalled if the current is lower than the predetermined value even at the highest driving frequency.

Display arrays of the type discussed are available in which the display elements or pixels have differing sizes and accordingly different capacitances. In such a case the means may be operative to compare the current flowing across a respective element with a predetermined value of current appropriate to that element. Alternatively the means may be operative to increase the frequency of the driving signal to a value appropriate to the size of element and to compare the current across each element with the same predetermined value of current.

A fault detection arrangement according to the invention can be applied both to displays of the direct drive type, where each pixel electrode is independently driven, and the multiplexed type, where electrodes for two or more pixels are connected together, selection of a pixel then being made by appropriate shaping of the driving waveform.

In another aspect the invention provides a method for checking for the presence of faults in a liquid crystal display element having a pair of opposed electrodes across which an a.c. driving signal is applied, the method comprising increasing the frequency of the driving signal and comparing the current flowing between the electrodes with a predetermined value.

In order that the invention may be better understood embodiments thereof will now be described by way of example with reference to the accompanying drawings, in which;

Figure 1 is a partly schematic circuit diagram of a fault detection arrangement according to the invention;

Figure 2 shows the interconnection arrangement between two liquid crystal elements disposed in parallel; and

Figure 3 is a circuit diagram showing the interconnection arrangement for a display array where each element has a common backplane.

Figure 1 shows two character arrays 1 each comprising a 7 x 5 matrix of liquid crystal elements or pixels 2. Although not shown, a light source is disposed behind each of the elements which may then be selectively switched between opaque and transparent states to shutter the light sources and display a character.

Each pixel element 2 comprises liquid crystal material sandwiched between a pair of electrodes 2a, 2b. Each array 1 has an associated driver integrated circuit (I.C.) 3, to which the electrodes 2a, 2b are attached, and which is connected to and controlled by a microprocessor 4. The a.c. frame input, data signal, clock signal and load signal are fed to each driver circuit on a respective databus 5.

The power supply unit (P.S.U.) 6 provides the power connections for each driver circuit 3. V_{cc}/V_{dd} and 0v signals are provided on line 7, while $-V_{ee}/-V_{ss}$ signals are provided on line 8. Each driver circuit 3 has an associated switch 9 connected by means of a buffer 10 to the microprocessor 4 by which the $-V_{ee}/-V_{ss}$ signals on line 8 of the P.S.U. 6 can be supplied selectively to each driver circuit 3.

Within each driver circuit 3, logic current flows between V_{dd} and 0V establishing the status of and updating the shift registers and other logic components. In addition, power current flowing between V_{cc}/V_{dd} and $-V_{ee}/-V_{ss}$ flows within the output stages of each driver circuit 3 and through the LCD elements 2 being driven. In order to sample the current flowing across an LCD element 2, a sampling resistor 11 is connected within line 8. The sampling resistor 11 is of sufficiently high value to drop a measurable voltage under load corresponding to one pixel on one driver circuit 3 when the frame

signal is driven at an increased frequency, as will be explained later on. A diode 12 disposed in parallel to the resistor limits the dropped voltage so as not to reduce the voltage applied to the driver circuit 3 by an excessive amount. The voltage dropped across the resistor 11 is amplified by a d.c. amplifier 13, the output of which is connected through a sample and hold circuit 14 to a comparator 15. The comparator 15 sends a signal to the microprocessor 4 when two signals received sequentially from the sample and hold circuit 14 differ by an amount equal to that supplied by the reference voltage device 16.

At a time when the sign is not required to display a message, the microprocessor 4 enters a test mode. This may be done on a periodic basis determined by the microprocessor 4, or on command from an external host system. Firstly the switches 9 are activated to disable all the driver circuits except the one to be tested. The microprocessor 4 then raises the frame frequency to a value at which the highest capacity cell within the system would just fail to trigger the comparator 15. This frequency value can be determined empirically so as to obtain a current value greater than the quiescent current of the driver, but not so large as to be dependent significantly on the drivers' output impedance. All the pixel elements 2 in the selected driver circuit are reset to the off condition. After a short stabilisation period, the sample and hold circuit 14 is energised and the quiescent current value is then applied to the input of the d.c. amplifier 13. After that, the microprocessor 4 causes the driver circuit 3 to energise one pixel element 2 only and the current flowing on line 8 is then compared to the prevailing quiescent value, the comparator 15 providing an output if they differ by a predetermined amount. If the comparator has not triggered, the

frequency is increased step wise to a maximum value until either the comparator has triggered or the frequency has reached a level at which the lowest capacitance cell within the system would have triggered the comparator.

If the comparator 15 triggered at the lower frame frequency limit, the respective LCD pixel element 2 is confirmed as faulty due to a full or partial short circuit. If the comparator has not triggered even at the upper frequency limit then the respective LCD element (or the interconnecting tracks) is confirmed as faulty due to a full or partial open circuit connection. If the comparator triggers at an intermediate frequency value then the respective LCD element is confirmed as being functional.

Each pixel element within each character array can be tested sequentially, any fault being logged within the microprocessor 4 for reporting to the host system.

The upper and lower limits of frequency can be determined empirically, different ranges being used for different sized pixel elements. This avoids the need for separate current thresholds, however, these may be provided instead, using the same frequency range for different sized elements. For large area (high capacity) LCD pixel elements, such as may be used in large outdoor displays, the sample and hold circuitry 14 may be omitted as the display current drawn on correctly operational pixels may be considerably higher than the quiescent current of the associated driver circuit. This may also be the case where the driver circuit has a particularly stable quiescent current. Under such conditions, current drawn is sampled as a reference voltage using a d.c. amplifier and the output compared directly with a reference voltage.

Figure 2 shows an arrangement where two LCD elements 2_1 , 2_2 are disposed one in front of the other. The frontmost electrodes 2_{a1} , 2_{a2} of each element are connected together as are the rearmost electrodes 2_{b1} , 2_{b2} . The fault detection arrangement is the same as that shown and described with reference to Figure 1. A further test may be carried out for such pixel arrangements by having further frequency ranges to establish whether one cell in the arrangement has failed, or in the connection to the combined arrangement. In the case of two elements of differing sizes or types it is possible, by having two frequency ranges, to determine which has failed.

Figure 3 shows a character array 1, which is similar to the separate LCD element system described with reference to Figure 1, except that each pixel element 2 has a common electrode or backplane 20 which is driven from either a dedicated back plane output on the driver circuit 3 or, as shown, by a plurality of segment driver lines connected to the backplane 20 by means of respective limiting resistors 23, 24, 25. In this way circulating currents between the output stages of the driver circuit 3 upon power up and/or in the event of data errors are minimised. With such arrangements the common electrode 20 is driven by a multiplexed signal, the difference in optical performance between the pixels being controlled by appropriate shaping of the waveforms applied to the backplane 20. Such arrangements can be tested in the same way as that described with reference to Figure 1.

Driver circuits are available which can be configured for both the multiplex drive shown in Figure 3 and for direct drive (i.e. that shown in Figure 1 where each electrode for each pixel is connected independently to the driver circuit). With such a device a

further mode can be selected during testing where two pixels effectively form a single pixel of twice the area enabling tests to be performed in a similar manner to that described with reference to Figure 1 as if half the number of pixels existed on the display. A possible fault condition is an interconnect break between the two pixels on one external segment connection. In the test described previously this would be logged as an open circuit fault. However by further increasing the frame frequency it is possible to establish whether the open circuit applies to one or both pixels.

Under some circumstances an open circuit fault, for example, due to electrode erosion, can be associated with high capacitance leakage around the display electrodes. This can mean that a faulty display can pass the previously mentioned tests. In order to account for this possibility an extra test can be applied which makes use of the dielectric anisotropy of liquid crystals i.e. that the capacitance across a fault free L.C.D. cell will vary according to the voltage applied across it, whereas the capacitance due to leakage around the cell will not. Therefore the drive circuitry may be also arranged, whilst at the elevated frame frequency, to drive the L.C.D. cell at at least two drive voltages both above and below the liquid crystal operating knee and to monitor the current flowing across the cell in the way previously described.

CLAIMS

1. A fault detection arrangement for a liquid crystal display element having a pair of opposed electrodes across which an a.c. driving signal is applied, the arrangement comprising means for increasing the frequency of the driving signal and for comparing the current flowing between the electrodes with a predetermined value.
2. A fault detection arrangement according to claim 1 in which the means is operative to progressively change the frequency over a range of values.
3. A fault detection arrangement according to claim 2 in which the means is operative to signal a fault due to a full or partial short circuit upon detection of a current higher than the predetermined value at the lowest driving frequency, and to signal a full or partial open circuit fault if the current is lower than the predetermined value at the highest driving frequency.
4. A fault detection arrangement according to any preceding claim for a plurality of liquid crystal display elements, each element defining a pixel of a character display.
5. A fault detection arrangement according to claim 4 for liquid crystal display elements of differing sizes and in which the means is operative to compare the

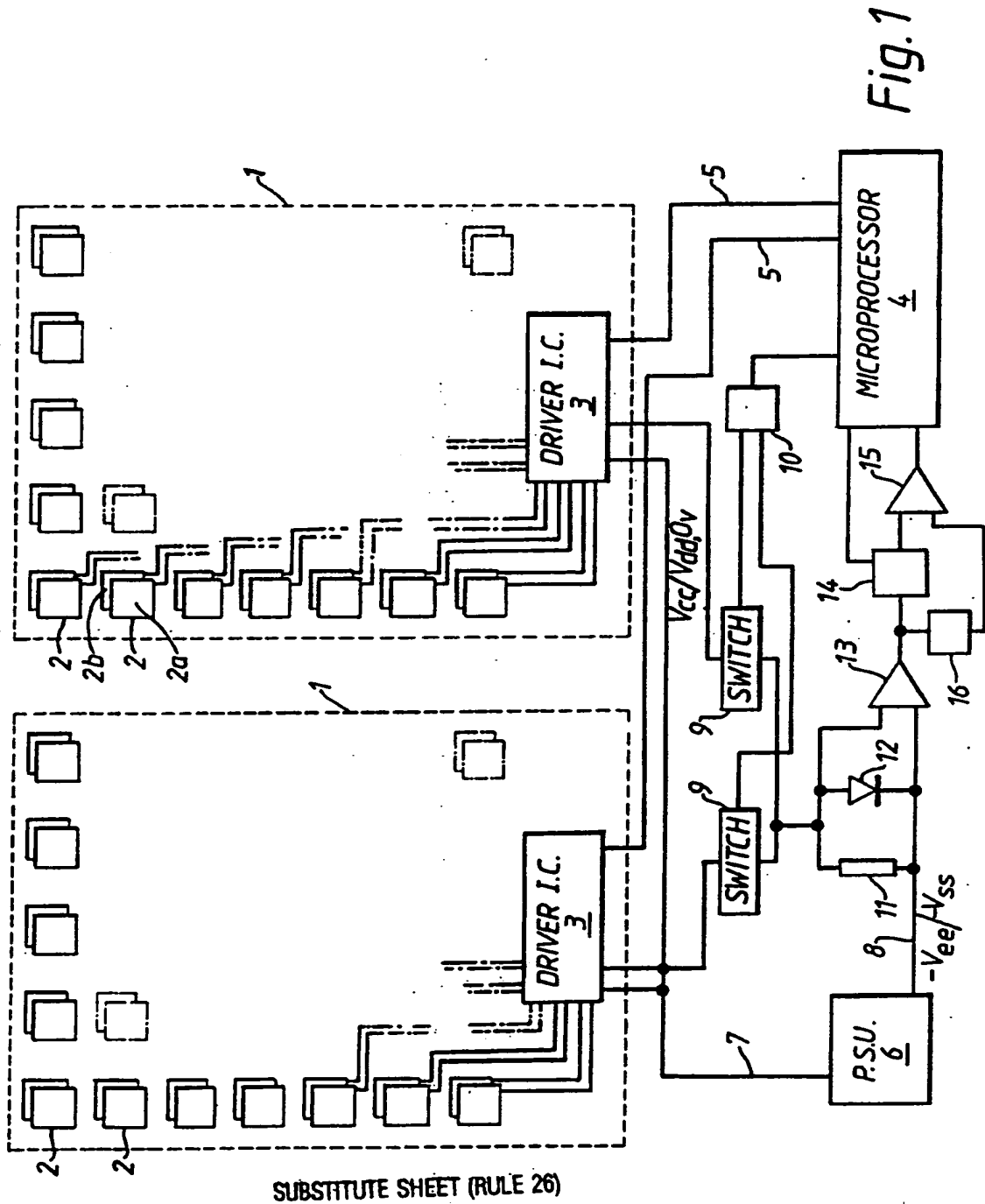
current flowing across a respective element with a predetermined value of current appropriate to that element.

6. A fault detection arrangement according to claim 4 for liquid crystal display elements of differing sizes and in which the means is operative to increase the frequency of the driving signal to a value appropriate for the size of element and to compare the current flowing across each element with the same predetermined value of current.
7. A fault detection arrangement according to claim 4 for a display system comprising a plurality of arrays of pixels, each array having an associated driving circuit, the fault detection arrangement including means for isolating each driving circuit and being operative to sequentially test each pixel within a respective array.
8. A fault detection arrangement according to claim 7, in which a quiescent current from the driving circuit is used as a reference against which the current flowing through a pixel element is compared.
9. A fault detection arrangement according to claim 8 in which the quiescent current is sampled before each pixel element is tested.
10. A fault detection arrangement according to any preceding claim including a resistor for sampling the current flowing between the electrodes, an amplifier for

amplifying the voltage dropped across the resistor, and a comparator for comparing the amplified voltage with a predetermined reference voltage.

11. A fault detection arrangement according to claim 9 or 10, including sample and hold circuitry, the arrangement being operative to sample the quiescent current, sample a pixel current, the comparator then being operative to compare the difference between the two current values with a predetermined reference value and to generate a signal if the difference value exceeds the reference value.
12. A fault detection arrangement according to claim 4 in which two or more pixel elements share a common electrode.
13. A fault detection arrangement according to any preceding claim comprising means for varying the voltage of the a.c. driving signal and for comparing the current flowing between the electrodes at at least two different voltage levels.
14. A method for checking for the presence of faults in a liquid crystal display element having a pair of opposed electrodes across which an a.c. driving signal is applied, the method comprising increasing the frequency of the driving signal and comparing the current flowing between the electrodes with a predetermined value.

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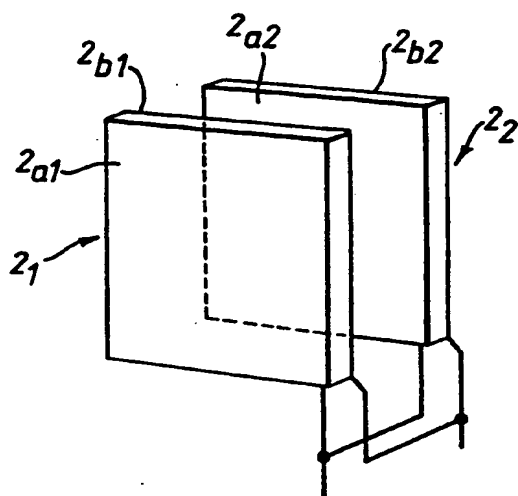


Fig. 2

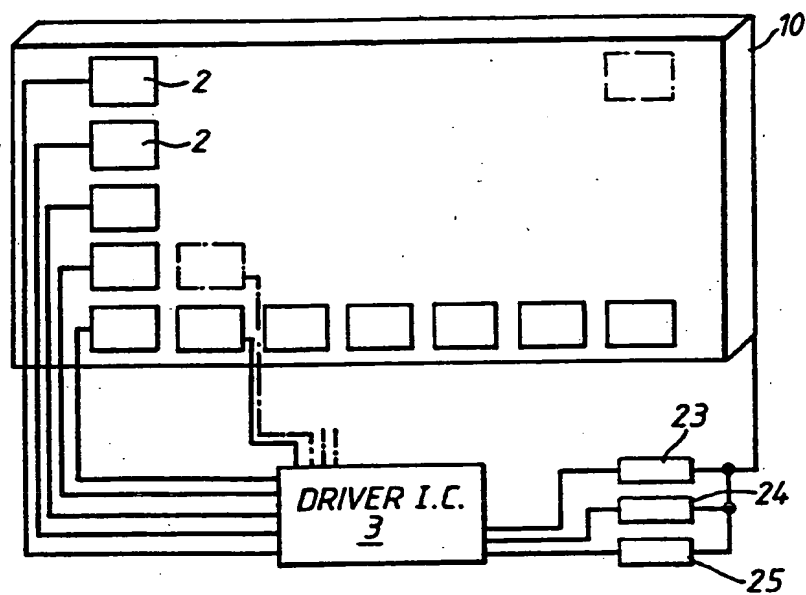


Fig. 3

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INTERNATIONAL SEARCH REPORT

Interns Application No
PCT/GB 94/02550

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 G01R31/28 G02F1/13

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 6 G01R G02F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	FR,A,2 680 595 (SATAM) 26 February 1993 see page 3, line 35 - page 4, line 38; figures 1-4	1,3,4, 7-10,12, 14
A	WO,A,80 00038 (METTLER INSTRUMENTE) 10 January 1980 see page 2, line 8 - page 3, line 5 see page 4, line 21 - page 6, line 31; figures 1-3	1,4,7,9, 12,14
A	PATENT ABSTRACTS OF JAPAN vol. 4, no. 100 (P-019) 18 July 1980 & JP,A,55 059 347 (HITACHI) 2 May 1980 see abstract	1,10,14

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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14 March 1995

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INTERNATIONAL SEARCH REPORT

Information on patent family members

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
FR-A-2680595	26-02-93	NONE	
WO-A-8000038	10-01-80	CH-A- 627575	15-01-82
		EP-A,B 0015914	01-10-80
		US-A- 4311993	19-01-82

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